

Amendments to the Specification:

Please replace paragraph [0007] with the following amended paragraph:

[0007] When the master clock 103 goes low that data is held by the master storage node 104. When the slave clock (109, 111) goes high, pass devices 108 and 112 allow data to pass. The data stored in storage node 104 propagates through inverter 114, through pass device 108 to storage node 106 and through pass device 112 to storage node 110. As a result of inverter 114 each individual storage node nodes 106 and 110 will store an opposite value.

Please replace paragraph [0008] with the following amended paragraph:

[0008] When the slave clock (109, 111) goes low, the two values stored in the storage nodes 106 and 110 are held independently of each other and propagated to the output Q 116 and the compliment of the output Qn 120. The data is then inverted using inverters ~~114~~ 115 and 118, respectively and output at output node Q 116 and the compliment of output node Qn 120.

Please replace paragraph [0014] with the following amended paragraph:

[0014] A circuit, comprises an input conveying an input signal; a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal; a first storage node coupled to the first pass gate and storing the first signal; a second pass gate coupled to the first storage node and enabling a second signal in response to the first signal stored in the first storage node and in response to a slave clock signal, wherein the slave clock generates a compliment to the clock signal; a first inverter coupled to the first storage node and generating a first inverted signal in response to the first signal stored in the first storage node; a third pass gate coupled to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and a second storage node coupled to the second pass gate and coupled to the third pass gate, the second storage node storing the second signal and the third signal.

Please replace paragraph [0015] with the following amended paragraph:

[0015] A method of operating a differential register, the differential register comprising an output node, a complimentary output node and a storage node coupled between the output node and the complimentary output node, the method comprises the steps of storing a first value in the storage node; storing the compliment of the first value in the storage node; and on power-up, conveying

the first value stored in the storage node out of the output node and conveying the compliment of the first value stored in the storage node out of the ~~compliment of the~~ complimentary output node.

Please replace paragraph [0024] with the following amended paragraph:

[0024] When the master clock 204 transitions low and the slave ~~clock~~ clocks 210 and 216 transition high the value stored in storage node 206 propagates through the remainder of the circuit. For example, when the slave clock 210 transitions high the pass device 208 operates and the value in storage node 206 propagates and is stored in storage device 218. When the slave clock 216 transitions high, the pass device 214 operates and the value in storage node 206 is inverted in inverter 212 and then stored in storage node 218. It should be appreciated that in one embodiment of the storage node 218 a separate device and/or combination of devices are used to store signals propagated through pass device ~~218~~ 208 and pass device 214. The signal propagated through pass device 208 is inverted in inverter 220 and output through output node Q 222. The signal propagated through pass device 214 is inverted in inverter 224 and output through the compliment of output node Qn 226.